REMARKS

Claims 1-18 are pending in the present application.

Drawings

Applicant notes the Examiner's acceptance of the Replacement Drawing as submitted along with the Amendment dated August 3, 2006.

Claim Rejections-35 U.S.C. 103

Claims 1-18 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tuda et al. reference (U.S. Patent No. 5,132,937) in view of the Kono et al. reference (U.S. Patent No. 5,455,536). This rejection is respectfully traversed for the following reasons.

The circuit for detecting an abnormal operation of memory of claim 1 includes in combination a delay circuit "for delaying an output data output from the memory for a predetermined period of time and for outputting a delayed data responsive thereto"; and a comparison circuit "for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

As previously emphasized in the Remarks section of the Amendment dated August 3, 2006, Applicant respectfully submits that the Examiner has failed to clearly

explain how the Tuda et al. reference may be interpreted to include the delay circuit as featured in claim 1. In column 4, lines 2-41 of the Tuda et al. reference as specifically relied upon, both delay circuit 212 of Fig. 3A and inversion delay circuit 211a of Fig. 3C are described. In contrast, column 6, lines 31-58 of the Tuda et al. reference as specifically relied upon provides description of Fig. 6. That is, the Examiner has not specifically identified which element of the Tuda et al. reference has been interpreted as the delay circuit of claim 1.

Particularly, delay circuit 212 in Fig. 3A of the Tuda et al. reference is described in column 4, lines 6-8 as delaying **an ATD pulse which is an output of address change detecting circuit 211.** Delay circuit 212 of the Tuda et al. reference is not described or even remotely suggested as delaying an output data output from a memory, as would be necessary to meet the features of claim 1. Inversion delay circuit 211a as shown in Fig. 3C of the Tuda et al. reference delays column address signal Adc and row address signal Adr. The Tuda et al. reference as relied upon does not disclose or suggest a delay circuit that delays an output data output from memory, as would be necessary to meet the features of claim 1.

The above noted arguments were presented in the paragraph bridging pages 17-18 of the Amendment dated August 3, 2006. The Examiner has made the current Office Action final, but has failed to address these arguments on the record, contrary to the guidelines as set forth in Manual of Patent Examining Procedure sections 707.07(f) and 706.07. The final Office Action should thus be considered as improper for at least

these reasons.

With further regard to this rejection, the Examiner has secondarily relied upon the Kono et al. reference as apparently disclosing a comparison circuit "for outputting a not-coincident signal from carrying out a comparison between the data and the delayed data". That is, the Examiner has apparently interpreted delay 22 in Fig. 3 of the Kono et al. reference as equivalent to the delay circuit of claim 1.

However, as described beginning in column 4, line 21 of the Kono et al. reference with respect to Fig. 3, a received IF signal is input to demodulator 12, which executes coherent demodulation of the received IF signal and thus outputs received data S_0. Delay 22 delays input received data S_0 and provides the corresponding delayed signal to comparator 24 as S_2, whereby comparator 24 performs comparison between corrected data S_1 and delayed data S_2 at a timing controlled by clock CL. **Delay 22 in Fig. 3 of the Kono et al. reference does not delay an output data output from a memory.** This should be particularly clear because the Kono et al. reference is concerned with demodulation, not with detecting abnormal operation of a memory. Delay 22 in Fig. 3 of the Kono et al. reference therefore cannot be interpreted as the delay circuit of claim 1. Moreover, one of ordinary skill would have no motivation to modify the semiconductor memory device of the Tuda et al. reference in view of the demodulator of the Kono et al. reference, because the teachings are clearly from divergent, unrelated fields. As such, the Kono et al. reference does not overcome the above noted deficiencies of the primarily relied upon Tuda et al. reference. Applicant

therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1-7 is improper for at least the above reasons.

With further regard to this rejection, since the Tuda et al. and Kono et al. references do not disclose a delay circuit for delaying an output data output from memory, the prior art as relied upon by the Examiner clearly does not disclose or even remotely suggest a comparison circuit that compares output data output from a memory with output data from a memory that is delayed, to provide a non-coincidence signal as would be necessary to meet the further features of claim 1. Applicant therefore respectfully submits that the circuit for detecting an abnormal operation of memory of claim 1 would not have been obvious over the prior art as relied upon by the Examiner, taken singularly or together, and that this rejection of claims 1-7 is improper for at least these additional reasons.

With regard to claim 2, the Examiner has very generally asserted that column 4, lines 45 through to column 5, line 25 and Fig. 6 of the Tuda et al. reference **explicitly** teach that an access speed of a memory is detected. However, as asserted in the Amendment dated August 3, 2006, the above noted portions of the Tuda et al. reference as relied upon do not specifically or explicitly describe, mention, or consider access speed of a memory, or more particularly detection thereof. In contrast, a result storing mode is described in column 5 of the Tuda et al. reference. Applicant therefore

respectfully submits that claim 2 would not have been obvious in view of the prior art as relied upon, and that this rejection of claim 2 is improper for at least these additional reasons.

Regarding claim 3, since the Tuda et al. reference as relied upon by the Examiner does not disclose a comparison circuit that outputs a non-coincidence signal based on comparison of output data from a memory with output data from a memory that is delayed. The Tuda et al. reference clearly does not explicitly or otherwise teach a circuit that holds address information in the case of non-coincidence in response to a non-coincidence signal, as asserted by the Examiner.

Regarding claim 6, column 4, lines 2-41 and column 5, lines 67 through to column 6, lines 3 of the Tuda et al. reference do not explicitly or otherwise teach that delay circuit 212 in Fig. 3A has a delay time that can be adjusted, as would be necessary to meet the features of claim 6.

These above noted arguments with respect to claims 2, 3 and 6 have been presented in the previous Amendment dated August 3, 2006. The Examiner has however failed to address these arguments in the Final Office Action dated October 16, 2006. **Applicant therefore respectfully submits that the Final Office Action dated October 16, 2006, is incomplete in this respect and thus improper.**

The integrated circuit of claim 8 includes in combination a memory; a delay circuit "which delays an output data from the memory and outputs a delayed data responsive thereto"; and a comparison circuit "which compares the output data from the

memory and the delayed data, and which outputs a noncoincidence signal when the output data and the delayed data are not coincident".

As asserted above with respect to claim 1, the delay circuit 212 in Fig. 3A of the Tuda et al. reference delays an ATD pulse output from address change detecting circuit 211, **not data output from a memory**, as would be necessary to meet the features of claim 8. Moreover, address change detecting circuit 211 has input thereto column address signal Adc and row address signal Adr, and therefore does not compare output data from a memory with output data from a memory that is delayed, as would be necessary to meet the further features of claim 8. The Kono et al. reference as relied upon does not overcome these deficiencies. Applicant therefore respectfully submits that claim 8 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 8, 17 and 18 is improper for at for at least these reasons.

With further regard to this rejection, the Tuda et al. reference does not appear to include first and second latch circuits as featured in claim 17. With regard to claim 18, the Tuda et al. reference does not provide a noncoincidence signal as featured, and thus does not include an address information storing circuit which stores address information when a noncoincidence signal is output by a comparison circuit.

Applicant also respectfully submits that the method for detecting an abnormal operation of memory of claim 9 would not have been obvious in view of the relied upon prior art for at least somewhat similar reasons as set forth above with respect to claim

1. Particularly, delay circuit 212 in Fig. 3A of the Tuda et al. reference does not delay an output data output from a memory. Also, address change detecting circuit 211 in Fig. 3A of the Tuda et al. reference does not output a noncoincidence signal based on comparison of output data output from a memory with output data from a memory that is delayed. The Kono et al. reference as relied upon does not overcome these deficiencies. Applicant therefore respectfully submits that the method for detecting an abnormal operation of memory of claim 9 would not have been obvious in view of the prior art as relied upon taken singularly or together, and that this rejection of claims 9-16 is improper for at for at least these reasons.

With further regard to this rejection, Applicant respectfully submits that the Tuda et al. reference as specifically relied upon does not detect access speed of memory as featured in claim 10, and does not hold address information in case of noncoincidence in response to a noncoincidence signal as featured in claim 11. Moreover, since delay circuit 212 in Fig. 3A of the Tuda et al. reference is not described as having adjustable delay time, the Tuda et al. reference does not disclose the features of claim 15. The Kono et al. reference as relied upon does not overcome these deficiencies. Applicant therefore respectfully submits that claims 10, 11 and 15 would not have been obvious for at least these additional reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the

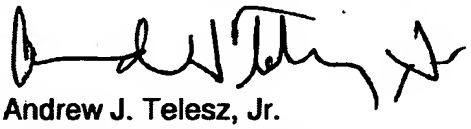
corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE & WHITT, P.L.L.C.



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